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Modeling Temperature Response Profile of MOSFET Chip with Heat Sink Parameters in Power Inverters

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Abstract: Direct current to alternating current converter is applied in the conversion of renewable energy such as solar and wind energy. The switching operation is performed by metal oxide semiconductor field effect transistor chips (MOSFET), during the operation heat is generated and if the heat generated is not properly dissipated, it may lead to thermally induced failure. This research modelled the temperature profile of the MOSFET chip with geometrical properties of the heat sink to which they are attached. The model was implemented in a MATLAB environment to obtained optimal heat sink parameters which was solved numerically with ANSYS and experimentally tested in a 1.6 kW inverter. The maximum MOSFET temperature obtained analytically, numerically and experimentally are is 73.68°C, 81.44°C and 87.35°C at a pulse load of 1000W. The numerical and experimental results of the optimized heat sink temperatures show good correlation with 7% deviation at a pulse load of 1000W and an average deviation of 17% in the power range of 600W to 1000W which shows that the optimized heat sink for the MOSFET chips work well and the model can be deploy for rapid prototyping of power inverter.

Keywords: Temperature; Heat sink; MOSFET chips; Thermal failure; Pulse load.

1. Introduction

Recent years have seen a rise in the quest to find renewable energy sources with diminishing strata of hydrocarbon fuels. To use these renewable energy resources, a DC to AC converter is important [1]. The most frequently used semiconductors in DC to AC converters is the metal oxide semiconductor field effect transistor (MOSFET), which convert power from DC to AC [2]. The materials used in fabrication of the semiconductor module have different coefficient of thermal expansion under different temperature conditions which can lead to a reduction of lifetime or failure of the semiconductor, if thermal stress induced is not properly dissipated [3]. Due to the increasing portability of electronic devices the space available for heat dissipation is reduced which leads to an increase in the thermal load of the electronic device, thus the need for a thermal management system such as an heat sink to optimize the system within the limited space available and to guarantee the device works within safe temperature limits [4-5]. In order to reduce their temperature, heat sinks are typically used for heat dissipation from hot surfaces into a fluid in motion to quickly dissipate the heat effectively and continuously as this help improve power handling capability, reliability [6-7].

Arularasan and Velraj [8] analysed the application of heat sinks in the cooling of electronic devices using CFD (Computational Fluid Dynamics) to model and simulate the optimum parameters for a parallel plate heat sink such as fin height, fin thickness,

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base height and fin pitch. 'The optimal geometric parameters obtained for the fin height, fin thickness, base height and fin pitch were 48 mm, 1.6 mm, 8 mm and 4 mm respectively for an efficient heat sink design. Boopalan et al [9] optimized the best location for power electronic components with heat sink in order to reduce the overall temperature of a Hybrid Electrical Vehicle (HEV) inverter with the Insulated Gate Bipolar Transistor's (IGBTs) and diodes heat transfer models executed in MATLAB environment. Results showed that the temperature of the inverter decreased by 5°C and the total heat sink length reduced by 15.9 cm.

Castelan et al [10] worked on implementing a model of forced-air cooling system to be used in the design process of a heat sink, a model was built using fluid dynamics to account for the relationship between the fan and the heat sink and the heat exchange between the fins and the forced air generated by the fan. The developed model was experimentally verified using a custom heat sink built for this process, and the effect of various parameters, such as fan power, heat sink dimensions and materials were investigated. The results obtained showed that both short and long heat sinks have a low performance index and therefore an optimum heat sink size is required to optimize the performance index, depending on the characteristics of the fan.

Kumar et al [11] worked on the design and selection of a heat sink that satisfies the required thermal and geometric criterion, and analysed the parameters that affected the heat-sink performance, and the overall performance of the system. Two types of heat-sink designs were experimentally tested a heat sink with one cut and a heat sink without cut for different heat inputs, from the experimental testing it was concluded that the heat sink with the cut had more temperature variations when compared to the heat sink without the cut. Liang et al [12] focused on finding the optimal design parameters such as fin height, fin number, fin thickness of a plate-fin heat sink under natural convection using the particle swarm optimization (PSO) Algorithm minimization written in MATLAB. The optimized heat sink results for the fin height, number of fins, fin thickness, base temperature were 44.8 mm, 25, 0.6 mm and 342.6241 K respectively.

Mjallal et al [13] investigated the effects of heat on electronic devices, how it increased their failure rates, and how most electronic devices use cooling mechanisms that typically consist of a metal heat sink cooled using either the active cooling method or the passive cooling method. The simulation was carried out using the ANSYS fluent simulation tool, by simulating the temperature variation of the heat sink walls as a function of time under active and passive cooling methods and comparing the results obtained, it was determined that active cooling greatly decreases the temperature of the heat sink. Mohan and Govindarajan [14] focused on investigating theoretically and experimentally the thermal efficiency of various forms of heat sinks. The heat sinks were modelled using a computational fluid dynamics code fluent, the experimental results obtained for the various heat sink geometries were compared to those predicted by the computational fluid dynamics code fluent. The results obtained showed improvement in heat transfer by increasing fin thickness up to 25% in 5 mm baseplate and up to 10% in 2.5 mm base plate thickness heat sink models.

Onoroh et al [15] modelled IRF 3205 MOSFET chips junction temperature using the concept of Cauer to Foster network synthesis. The transformation algorithm was based on Continuous Fraction Expansion with recursive relation, the model was optimized with MATLAB and results obtained from the thermal model and experimental testing were 34.7°C and 36.5°C respectively. From the literature review, a way of analytically determining the thermal response of the MOSFET chip with heat sink geometrics has not been well documented, thus this research modelled the temperature profile of MOSFET chips with heat sink parameters, the heat sink was optimized and then solved numerically and experimentally.

2. MOSFET Chips Thermoelectric Response with Heat Sink

Figure 1 depicts the geometry of a heat sink to which MOSFET chips are attached for the purpose of thermal dissipation.

The heat dissipated by the MOSFET chips, consists of electrical conduction losses, switching losses and thermal conduction losses and can be expressed as:

$$Q = F_{sw}\left[(R_{Dson} \times I^2{}_{Drms}) + \left(E_{on} + E_{off}\right)F_{sw} + k\frac{dT}{dx}\right] \qquad (1)$$

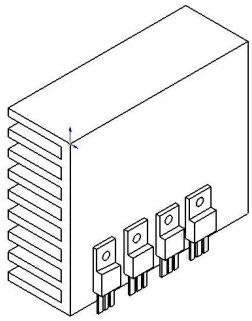

Figure 1: Heat Sink Model of Power Inverter

The switch ON energy losses and switch OFF energy losses are given equation (2) and equation (3) respectively.

$$E_{on} = U_{DD} \times I_{Don} \times \frac{t_{ri} + t_{fu}}{2} + Q_{rr} \times U_{DD} \quad (2)$$

$$E_{off} = U_{DD} \times I_{Doff} \times \frac{t_{ru} + t_{fi}}{2} \quad (3)$$

Where R_{Dson} is the drain source on state resistance, Ω, I_{Drms} is the rms value of the MOSFET chip, A, F_{sw} is the switching frequency,Hz, k is the thermal conductivity, W/mK, dT/dx is the rate of temperature change with length, I_{Don} is the on state drain current, A, I_{Doff} is the off state drain current, A, U_{DD} is the inverter supply voltage,V, t_{ri} is the current rise time, ns, t_{ru} is the current fall time ns, t_{fi} is the voltage rise time, ns, t_{fu} is the voltage fall time, ns, Q_{rr} reverse recovery charge.

Application of Fourier's and Newtons laws yield the heat transfer across the heat sink as:

$$-\frac{d}{dx}\left(-A_c k \frac{dT}{dx}\right)dx - hPdx(T - T_\infty) = 0 \quad (4)$$

This reduces to the ordinary differential equation:

$$\frac{d^2T}{dx^2} - \frac{hP}{kA_c}(T - T_\infty) = 0 \quad (5)$$

The temperature can be made dimensionless as:

$$\theta = \frac{T - T_\infty}{T_b - T_\infty}$$

Upon re arrangement yields:

$$T = \mathrm{T}_\infty + (T_b - T_\infty)\theta \quad (6)$$

The length of the fin can be made dimensionless as:

$$X = \frac{dx}{L}$$

Upon re-arrangement gives:

$$dx = XL \quad (7)$$

Substituting equation (6) and equation (7) into equation (5) yields:

$$\frac{d^2}{d(XL)^2}(T_\infty + (T_b - T_\infty)\theta) - \frac{hP}{kA_c}((T_\infty + (T_b - T_\infty)\theta) - T_\infty) = 0 \quad (8)$$

Equation (8) upon simplification becomes:

$$\frac{d^2\theta}{dX^2} - \frac{hP}{kA_c} = 0 \quad (9)$$

Let

$$m^2 = \frac{hP}{kA_c} \quad (10)$$

Equation (9) becomes:

$$\frac{d^2\theta}{dX^2} - m^2\theta = 0 \quad (11)$$

Equation (11) is an ordinary differential equation, its complementary solution is:

$$\theta = Ae^{mX} + Be^{-mX} \quad (12)$$

Differentiation of equation (12) yields:

$$\frac{d\theta}{dX} = mAe^{mX} - mBe^{-mX} \quad (13)$$

The dT/dx in equation (1) can be made dimensionless as:

$$\frac{dT}{dx} = \frac{d\theta}{dX}\frac{(T_b - T_\infty)}{L} \quad (14)$$

Therefore, equation (1) becomes:

$$Q = -\left(F_{sw}\left[(R_{Dson} \times I^2{}_{Drms}) + \left(E_{on} + E_{off}\right)f_{sw} + k\frac{d\theta}{dX}\left(\frac{T_b - T_\infty}{L}\right)\right]\right) \quad (15)$$

Upon re-arrangement yields:

$$\frac{d\theta}{dX} = -\frac{\left[F_{sw}\left((R_{Dson} \times I^2{}_{Drms}) + \left(E_{on} + E_{off}\right)f_{sw} + Q\right)\right]L}{(T_b - T_\infty)k} \quad (16)$$

For the design of the heat sink, the temperature at the tip of the fin must be equal to the ambient temperature, therefore when X=1, θ=0, equation (12) becomes:

$$A = -Be^{-2m} \quad (17)$$

Applying the second boundary condition at X=0

$$\frac{d\theta}{dX} = -\frac{\left[F_{sw}\left((R_{Dson}\times I^2{}_{Drms})+\left(E_{on}+E_{off}\right)f_{sw}+Q\right)\right]L}{(T_b-T_\infty)k}$$

Equation (13) becomes:

$$-\frac{\left[F_{sw}\left((R_{Dson}\times I^2{}_{Drms})+\left(E_{on}+E_{off}\right)f_{sw}+Q\right)\right]L}{(T_b-T_\infty)k} = \\ = -mBe^{-2m+m(0)} - mBe^{-m(0)} \qquad (18)$$

Therefore:

$$B = \frac{\left[F_{sw}\left((R_{Dson}\times I^2{}_{Drms})+\left(E_{on}+E_{off}\right)f_{sw}+Q\right)\right]L}{e^{-2m}(T_b-T_\infty)km} \qquad (19)$$

In the light of equation (17), A becomes:

$$A = -\frac{\left[F_{sw}\left((R_{Dson}\times I^2{}_{Drms})+\left(E_{on}+E_{off}\right)f_{sw}+Q\right)\right]L(e^{-2m})}{(e^{-2m})(T_b-T_\infty)km} \qquad (20)$$

Substituting equation (19) and (20) into equation (12) gives:

$$\theta = -\frac{\left[f_{sw}\left(\left(R_{Dson}\times I^2_{Drms}\right)+\left(E_{on}+E_{off}\right)f_{sw}+Q\right)\right]Le^{(-2m)}.e^{mX}}{e^{-2m}(T_b-T_\infty)k} \\ +\frac{\left[f_{sw}\left(\left(R_{Dson}\times I^2_{Drms}\right)+\left(E_{on}+E_{off}\right)f_{sw}+Q\right)\right]Le^{-mX}}{e^{-2m}(T_b-T_\infty)km} \qquad (21)$$

Or

$$\frac{T-T_\infty}{T_b-T_\infty} = -\frac{\left[f_{sw}\left((R_{Dson}\times I^2{}_{Drms})+\left(E_{on}+E_{off}\right)f_{sw}+Q\right)\right]L}{e^{-2m}(T_b-T_\infty)km}\cdot \\ \cdot\left(e^{-2m+m\frac{x}{L}} - e^{-m\frac{x}{L}}\right) \qquad (22)$$

The MOSFET chip temperature profile model is:

$$T = \frac{\left[f_{sw}\left((R_{Dson}\times I^2{}_{Drms})+\left(E_{on}+E_{off}\right)f_{sw}+Q\right)\right]L}{e^{-2m}\cdot km}\cdot \\ \cdot\left(e^{-m\frac{x}{L}} - e^{-2m+m\frac{x}{L}}\right)+T_\infty \qquad (23)$$

The temperature profile can be expressed as a function of heat sink parameters using figure 2.

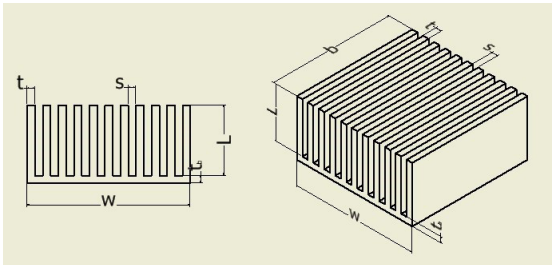

Figure 2: Heat sink geometry

The perimeter of the heat sink fins can be expressed as:

$$P = 2n(L+t) \qquad (24)$$

Where L is the length of the heat sink fin, m, t is the fin thickness m and n is the number of fins. The width of the heat sink is expressed as:

$$w = nt + (n-1)s \qquad (25)$$

Where s is the fin spacing, m. The convective heat transfer area is given as:

$$A_c = 2(L\times s)(n-1) \qquad (26)$$

In the light of equation (24) and equation (26), equation (10) becomes:

$$m = \sqrt{\frac{n(L+1)}{(L\times s)(n-1)}} \qquad (27)$$

Substituting equation (27) into equation (23), the temperature response profile of MOSFET chip as a function of heat sink parameters becomes:

$$T = \frac{\left[f_{sw}\left(\left(R_{Dson}\times I^2_{Drms}\right)+\left(E_{on}+E_{off}\right)f_{sw}+Q\right)\right]L}{e^{-2\sqrt{\frac{n(L+t)}{(L\times s)(n-1)}}}(T_b-T_\infty)k\sqrt{\frac{n(L+t)}{(L\times s)(n-1)}}}\cdot \\ \cdot\left(e^{-2\sqrt{\frac{n(L+t)}{(L\times s)(n-1)}}+\sqrt{\frac{n(L+t)}{(L\times s)(n-1)}}\frac{x}{L}} - e^{-\sqrt{\frac{n(L+t)}{(L\times s)(n-1)}}\frac{x}{L}}\right)+T_\infty \qquad (28)$$

Air properties are evaluated at mean temperature:

$$T_f = \frac{T_\infty + Tb}{2} \qquad (29)$$

The Raleigh's number is:

$$Ra = \frac{g\beta(T_h-T_\infty)w^3}{v^2}Pr \qquad (30)$$

Where Ra is Raleigh's number, Pr is Prandtl number,

v is kinematic viscosity m^2/s, $\beta = \frac{1}{T_f}(1/K)$. Nusselt's number Nu, is given:

$$Nu = 0.59Ra^{0.25} \quad (31)$$

It can also be expresses as [16]:

$$Nu = \frac{hl_e}{k} \quad (32)$$

Where l_e is Hydraulic diameter of the heat sink, obtained using the relation:

$$l_e = \frac{2(s \times L)}{(s + L)} \quad (33)$$

3. Methodology

This research modelled analytically the temperature of MOSFET chips as a function of geometrical properties of heat sink, the model was solved using MATLAB for pictorial representation of the temperature response profile to varying heat sink parameters at different load. The model was optimized and solved numerically using ANSYS FLUENT and thereafter tested experimentally for the purpose of validating the numerical results. The experimental setup as shown in figure 3 consists of a 2 KVA DC to AC converter, four 180 W solar panels in series and parallel connection, charge controller, four 100AH in parallel, DT-266 digital multi-meter and an MTM–380SD 3 Channels Temperature logger.

4. Results and Discussion

4.1. Analytical Results

4.1.1 Temperature Response Profile of MOSFET Chip against number of Fins and Fin Spacing

Figure 4 shows the plot of chip temperature profile versus number of fins and varying fin spacing at inverter load conditions of 600W, 800W, and 1000W respectively. The MOSFET temperature is seen to reduce with increasing number of fins and fin spacing, which can attribute to increase in convective surface area, similar results were obtained by Yazicioğlu and Yüncü [17] and Morrison [18]. From the results obtained it can be deduced that increasing the fin spacing improves the heat dissipation capability of the heat sink, thus lowering the temperature of the MOSFET chip and the temperature of the chip increases with an increase in pulse load due to the greater heat dissipation of the MOSFET chip as summarized in Table 1.

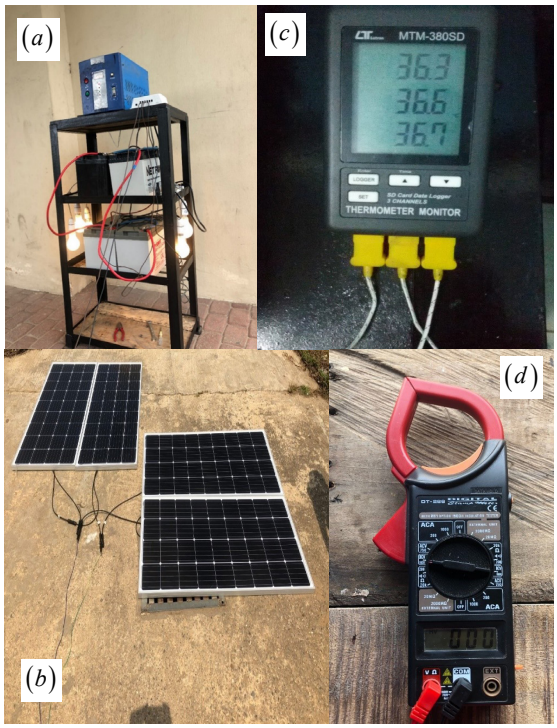

Figure 3: Experimental Setup. a. Inverter, battery and load assembly; b. Solar panel; c. MTM-380SD Temperature logger; d. Multimeter

4.1.2 Temperature Response Profile of MOSFET chip against number of Fins and Fin Thickness

Figure 5 shows the plot of chip temperature profile versus number of fins and varying fin thickness at inverter load conditions of 600W, 800W, and 1000W respectively. The MOSFET temperature is seen to reduce with increasing number of fins and increases with an increase fin thickness. Increase in fin thickness at constant number of fins tend to decrease the fin spacing and hence a reduction in convective area for heat dissipation. From the results obtained it can be deduced that decreasing the fin thickness improves the heat dissipation capability of the heat sink, thus lowering the temperature of the MOSFET chip and the temperature of the chip increases with an increase in pulse load due to the greater heat dissipation of the MOSFET chip as summarized in Table 2.

4.1.3 Temperature Response Profile of MOSFET chip against number of Fins and Fin Length

Figure 6 shows the plot of chip temperature profile versus number of fins and varying fin lengths at inverter load conditions of 600W, 800W, and 1000W respectively. The MOSFET temperature is

seen to decrease with increasing number of fins and fin length, which can be attributed to increase in convective surface area, similar results were obtained by Lee, [19] and Elnaggar, [20]. From the results obtained it can be deduced that increasing the fin length improves the heat dissipation capability of the heat sink, thus lowering the temperature of the MOSFET chip and the temperature of the chip increases with an increase in pulse load due to the greater heat dissipation of the MOSFET chip as summarized in Table 3.

From the analysis, it can be observed that there is an interdependency between the heat sink variables in helping to mitigate the effect of excessive heat on the chips and thus it becomes necessary to find the optimized geometric parameters which was performed using the FMINCON tool in MATLAB, to yield the optimized heat sink parameters detailed in table 4.

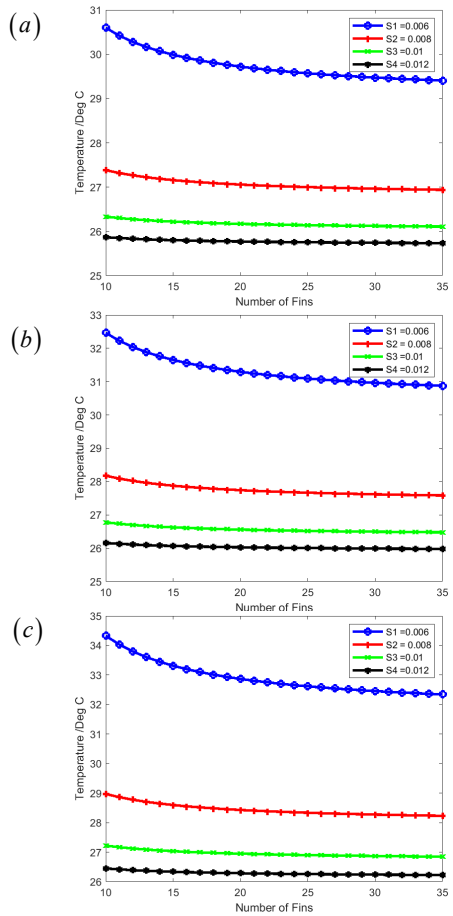

Figure 4: Chip Temperature Profile vs number of fins and fin spacing; a) 600W; b) 800W; c)1000W

Table 1: Maximum chip Temperatures with Loads

Load/W	*Max. chip temp./°C*	*% Change in chip temp.*
600	29.98	
800	31.65	5.57
1000	33.31	5.24

4.2 Temperature Contours of Heat Sink

The optimized heat sink was solved numerically using ANSYS fluent for pictorial representation of the temperature contours of the heat sink at different loads. Figure 7 shows the temperature contours at 600W, 800W and 1000W respectively. The temperature of the heat sink surfaces increases with an increase in pulse load as expected due to the greater heat dissipation of the MOSFET chip as summarized in Table 5.

4.3 Experimental Results

The experimental temperature profile of the optimized heat sink base is as shown in figure 8 at 600W, 800W, 1000W against time. The temperature is seen to increase with time and load as detailed in table 6. Table 7 high light the numerical and experimental maximum temperatures of the optimized heat sink with pulse load, clearly the percent deviation decreases with an increase in pulse load. It is reasonable to assume that the surface temperature of the heat sink base approximates the temperature of the MOSFET chip thus the chips are within the safe operating limit and thus the derived MOSFET chip temperature model is accurate enough to be used for rapid prototyping of power inverter systems.

5. Conclusion

A DC to AC converter is any electrical device that converts direct current to alternating current, it is used in a wide range of applications, during the switching operation by the MOSFET chip from DC to AC heat is generated which needs to be properly dissipated. This research modelled the temperature profile of a MOSFET chip with varying heat sink geometrical parameters for rapid prototyping of power inverter, with the aim of improving the heat dissipation to avert thermally induced failure. The optimized parameters for the heat sink fin length, number of fins, fin thickness, fin spacing derived model are: 0.015m, 15, 0.003m, and 0.012m respectively. The maximum MOSFET temperature obtained analytically, numerically

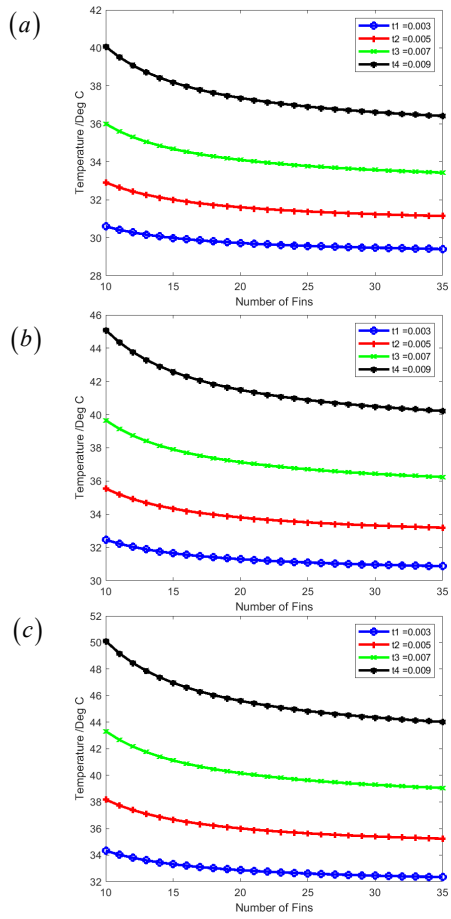

Figure 5: Chip Temperature Profile vs number of fins and fin thickness; a) 600W; b) 800W; c)1000W

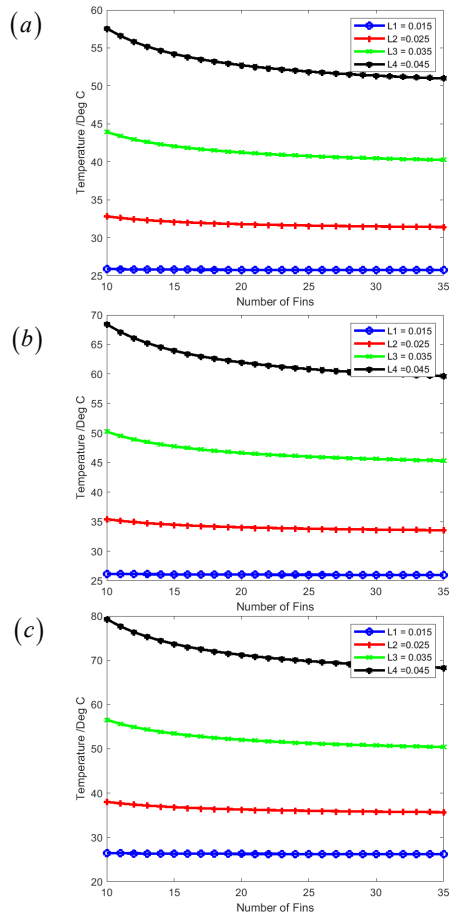

Figure 6: Chip Temperature Profile vs number of fins and fin length; a) 600W; b) 800W; c)1000W

Table 2: Maximum chip Temperatures with Loads

Load/W	*Max. chip temp./℃*	*% Change in chip temp.*
600	38.18	
800	42.57	11.49
1000	46.97	10.33

Table 3: Maximum chip Temperatures with Loads

Load/W	*Max. chip temp./℃*	*% Change in chip temp.*
600	54.20	
800	63.94	17.95
1000	73.68	15.23

Table 4: Optimized heat sink parameters

No of fins	*Fin thickness/m*	*Fin spacing /m*	*Length /m*
15	0.003	0.012	0.015

Table 5: Maximum chip Temperatures with Loads

Load/W	*Max. chip temp./℃*	*% Change in chip temp.*
600	47.06	
800	59.35	26.11
1000	81.44	37.21

Table 6: Maximum chip Temperatures with Loads

Load/W	*Max. chip temp./℃*	*% Change in chip temp.*
600	61.75	
800	72.60	17.57
1000	87.35	20.31

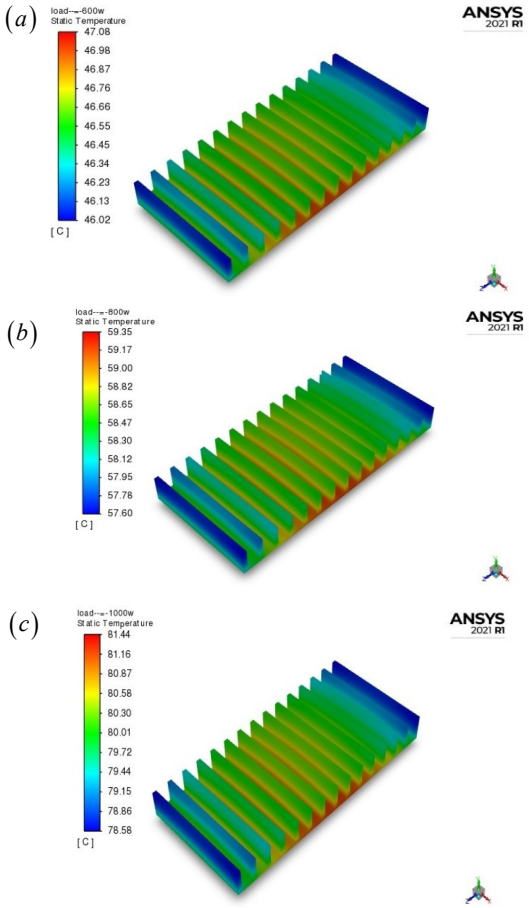

Figure 7: Heat Sink Temperature Contours; a) Temperature Contour at 600W; b) Temperature Contour at 800W; c) Temperature Contour at 1000W

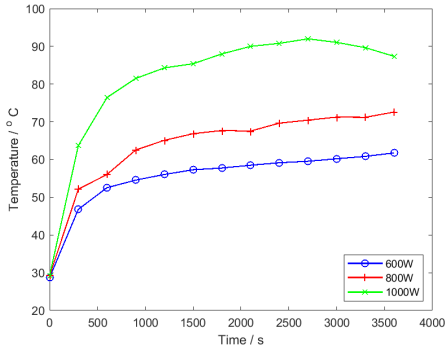

Figure 8: Experimental Heat Sink Temperature

Table 7: Comparison between Numerical and Experimental Temperatures of Optimized Heat Sink

Load/W	*Numerical temp./°C*	*Experimental temp./°C*	*% Deviation*
600	47.06	61.75	23
800	59.35	72.60	21
1000	81.44	87.35	7

and experimentally are 73.68oC, 81.44oC and 87.35oC at a pulse load of 1000W. The numerical and experimental results of the optimized heat sink temperatures show good correlation with 7% deviation at a pulse load of 1000W and an average deviation of 17% in the power range of 600W to 1000W which shows that the optimized heat sink for the MOSFET chips work well and the model can be deploy for rapid prototyping of power inverter.

References

1. Sarkar A., Issac B. (2016). Importance of Thermal Radiation from Heat Sink in Cooling of Three Phase PWM Inverter kept inside an Evacuated Chamber. Engineering Science and Technology, an International Journal, 20(2), pp. 1–10.
2. Musa A., Galadanci G.S.M. (2009). 5 K.V.A. Power Inverter Design and Simulation Based on Boost Converter and H-Bridge Inverter Topology. Bayero Journal of Pure and Applied Sciences, 2(1), pp. 6-13.
3. Cho S. E., Park S. J. (2010). Optimal Design of Heat sink for 3 Phase Voltage Source Inverter System by using Average Method. Modern Applied Science, 4(2), pp. 114-125.
4. Ekpu M., Bhatti R., Ekere N., Mallik S., Amalu E,. Otiaba K. (2011). Investigation of Effects of Heat Sinks on Thermal Performance of Microelectronic Package. 3rd IEEE International Conference on Adaptive Science and Technology (ICAST), Chatham Kent, United Kingdom, pp.127-132.
5. Prabhakar P.S., Ghuge N.C. (2015). Thermal Design and Analysis of Heat Sink Optimization and its Comparison with Commercially Available Heat Sink. International Journal of Engineering Research & Technology (IJERT), 4(12), pp. 210-216.
6. Onoroh F., Adewumi O. O., Ogbonnaya M. (2019). Characterization of a Finned Heat Sink for a Power Inverter. Journal of Physics: Conference Series: 1378 (022003), pp. 1-15.
7. Bar-Cohen A., Iyengar M., Kraus A.D. (2003). Design of Optimum Plate-Fin Natural Convective Heat Sinks. Journal of Electronic Packaging, 125, pp. 208-216.
8. Arularasan R., Velraj R. (2008). CFD Analysis in a Heat Sink for Cooling of Electronic Devices. International Journal of the computer, the Internet and Management ,16(3), pp.1-11.
9. Boopalan N., Ramasamy A.K., Nagi F.H. (2016). Power Electronics Component Location and Heat Sink Length Optimization Hybrid Electrical Vehicle (HEV). Indian Journal of Science and Technology,9(28), pp.1-6.
10. Castelan A., Cougo B., Brandelero J., Flumian D., Meynard T. (2015). Optimization of forced-air cooling system for accurate design of power converters. 24th IEEE International

Symposium on Industrial Electronics, Buzios, Brazil, pp. 367 – 372.

11. Kumar M., Kumar A., Kumar S. (2013). Optimum Design and Selection of Heat Sink. International Journal of Application or Innovation in Engineering & Management (IJAIEM), 2(3), pp. 541-549.
12. Liang C.H., Zeng S., Li Z. X., Yang D.G., Sherif S. A. (2016). Optimal Design of Plate-Fin Heat Sink under Natural Convection Using a Particle Swarm Optimization Algorithm. International Journal of Heat and Technology ,34(2), pp.275-280.
13. Mjallal I., Farhat H., Hammoud M., Ali S., Shaer A.A., Assi A. (2017). Cooling Performance of Heat Sinks Used in Electronic Devices. Conference Proceeding IEEE, Beirut Lebanon, pp.40-43.
14. Mohan R., Govindarajan P. (2011). Experimental and CFD analysis of heat sinks with base plate for CPU cooling. Journal of Mechanical Science and Technology, 25(8), pp.2003-2012.
15. Onoroh F., Enibe S. O., Adewumi O. O. (2018). Thermal Model and Experimental Validation of IRF 3205 MOSFET Switches for Inverter Application. FUW Trends in Science & Technology Journal 3(1), pp. 73-78.
16. Onoroh F.,Ogbonnaya M., Chukuneke J.L., Echeta C. B., (2018b). Thermal Optimization of Heat Sink for Inverter Applications. IOP Conference Series: Materials Science and Engineering, 413(012058), pp. 1-10.
17. Yazicioğlu B., Yüncü H. (2007). Optimum fin spacing of rectangular fins on a vertical base in free convection heat transfer. Heat and Mass Transfer, 44(1), pp.11–21.
18. Morrison A. T. (1992). Optimization of heat sink fin geometries for heat sinks in natural convection. Proceedings Intersociety Conference on Thermal Phenomena in Electronic Systems, pp. 145-148.
19. Lee S. (1995). Optimum Design and Selection of Heat Sinks. Eleventh IEEE SEMI THERM Symposium, Laconia, New Hampshire, pp. 48-54.
20. Elnaggar M.H. (2015). Heat Transfer Enhancement by Heat Sink Fin Arrangement in Electronic Cooling. Journal of Multidisciplinary Engineering Science and Technology (JMEST), 2(3), pp.457-460.